REMARKS/ARGUMENTS

Reexamination of the captioned application is respectfully requested.

A. SUMMARY OF THIS AMENDMENT

By the current amendment, Applicants basically:

1. Amend independent claims 1, 15, 21 and 35.
2. Editorially amend dependent claim 2.
3. Amend dependent claims 5, 15, 18 and 38.
4. Cancel claims 8-14 and 28-34 without prejudice or disclaimer.
5. Respectfully traverse all prior art rejections (*see* section B infra).
6. Request a one month extension of time.
7. Request consideration and official citation of prior art references (*see* section C infra).

B. PATENTABILITY OF THE CLAIMS

Original claims 1-40 stand rejected under 35 USC §102(b) as being anticipated by U.S. Patent 6,134,513 to Gopal. All prior art rejections are respectfully traversed for at least the following reasons.

Independent claims 1 and 21

Independent claims 1 (computer program product) and 21 (method) have been amended to include therein selected limitations of dependent claims 6 and 26, respectively. As amended, independent claims 1 and 21 both require that the step of solving the equation system further comprises: (a) rearranging equations in the equation system; (b) partitioning the admittance matrix into partitions; and (c) generating a simplified equation system based on the partitioning of step (b). As explained at least in part below, limitations of independent claims 1 and 21 are not taught or suggested by U.S. Patent 6,134,513 to Gopal.

U.S. Patent 6,134,513 to Gopal illustrates, in Fig. 3, a method for simulating a resistive circuit. The Fig. 3 steps of the method involve reading and translating an input list (step 302); compiling node information (step 304); detecting "floating" nodes (step

306); and finally computing a DC solution for the entire resistive circuit using a recursive technique (step 308). Various versions or "techniques" of the DC solution step 308 are described. As far as Applicants can surmise, the only DC solution version of even marginal interest is the matrix solution technique described with reference to Gopal Fig. 15 and Fig. 16. While the Gopal Fig. 15/ Fig. 16 matrix solution technique purports to involve an admittance model, Gopal does not teach or suggest limitations of Applicants' claims.

Gopal's description of the steps of Fig. 15 matrix solution technique is as follows:

> First, at step 1104 a sparse matrix is initialized. Next at loop 1106, for each resistor in the macro, step 1108 of stenciling an admittance model into the matrix is performed. The admittance model is arrived at by using the resistances, which are known, and the well known equation for admittance, and constructing a matrix according to well known techniques. The next loop in the process is loop 1110, in which step 112 of stenciling a y-parameter macromodel of an associated macro M_j into the matrix is performed for each instance J in the macro. Next, loop 1114 is performed, wherein step 1116, stenciling a voltage source model into the matrix, is performed for each terminal in the macro. Finally, the matrix is factored at step 1118 and the process is at end 1120.

Gopal's description is cryptic, referring blindly to "the well known equation for admittance" and "well known techniques" and inexplicably to "factoring". Apparently Gopal essentially "stencils" resistance values for each resistor and macro, and voltage source models, into a matrix such as that shown in Fig. 16. Gopal does not explain where any such stenciled value is placed, or how it corresponds to any equation. Yet it is clear that Gopal does not manipulate the matrix or perform actions such as those required by Applicants' claims. At best Gopal's logic is in selecting which values of the matrix to store (see col. 10, lines 24 – 58), rather than manipulating or partitioning the matrix in Applicants' claimed manner. Certainly Gopal does not (a) rearrange equations in the equation system; (b) partition the admittance matrix into partitions; or (c) generating a simplified equation system based on the partitioning of step (b).

Independent claims 15 and 35

Applicants' original independent claims 15 (computer program product) and 35 (method) have been amended to specify that plural types of connectivity blocks are inserted into the admittance matrix so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix. These and other limitations of independent claims 15 and 35 are not taught or suggested by U.S. Patent 6,134,513 to Gopal. For example, independent claim 15 and 35 specify, e.g., steps for generating an admittance matrix, including:

> generating a main circuit admittance block for a main circuit comprising the electrical circuit which is being analyzed;
>
> generating a subcircuit admittance block for a subcircuit comprising the electrical circuit which is being analyzed;
>
> inserting the main circuit admittance block and the subcircuit admittance block on a main diagonal of the admittance matrix;
>
> generating connectivity blocks which represent connectivity between the main circuit and the subcircuit;
>
> inserting the plural types of connectivity blocks so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix...

Even if a Gopal's "macro" were somehow construed as claimed subcircuit, Gopal does not explain where the macro is stenciled. The fact that Gopal's matrix is symmetric about its diagonal (col. 10, line 27 – 28) does not specify where Gopal places such a macro or any other element. Nor is there any hint that Gopal generates anything even akin to connectivity blocks which represent connectivity between a main circuit and a subcircuit. Indeed the spotty nature of Gopal's matrix and eagerness to eliminate entries confirms that Gopal has no such connectivity block entries. Certainly there is no teaching or suggestion that Gopal inserts anything like differing types of connectivity blocks symmetrically across a main diagonal of the Gopal matrix, particularly since Gopal seems to use only a lower triangle portion of his matrix anyway (see col. 10, line 27 – 31).

In the above regard, see also dependent claims 5, 12, 15, and 32 which refer to differing types of connectivity blocks which are symmetric with respect to one another about the main diagonal.

Dependent claims

Only selected aspects of Applicants' independent claim have been discussed above. Numerous ones of Applicants dependent claims have separate patentable merit. For example, dependent claims 3, 10, 20, 23, 30, and 40 specify that the electrical circuit has a telecommunications component including one of a multi-winded transformer, a loading coil, a line-driver, an analogue cable, and a filter. By contrast, Gopal refers exclusively to resistors, i.e., to the resistive network (associated with power distribution system). As such, Gopal's matrix must be symmetric. Applicants' solution allows inclusion of arbitrary electrical components such as e.g. transformers resulting in krakovians with arbitrary structure. This is exemplified in Applicants' Fig. 6 and Fig. 13.

C. INFORMATION DISCLOSURE STATEMENT (IDS)

1. The Examiner is respectfully referred to the Information Disclosure Statement (IDS) which was filed on May 10, 2005, and kindly requested to consider and officially cite the documents listed on the PTO-1449 attached to the Information Disclosure Statement (IDS) filed on May 10, 2005.

2. At various junctures[2] Applicants' specification refers to one or more of the following: (1) Analog Insydes, (2) *Mathematica* toolbox, and (3) MATLAB. Attached to this amendment is a PTO-1449 which lists several articles explanatory of one or more of (1) – (3). Copies of these articles are provided. It is requested that the Examiner consider and officially cite the documents listed on the PTO-1449 attached to this amendment.

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[2] See, for example, paragraphs [0006], [00071] of Applicants' specification.

D. MISCELLANEOUS

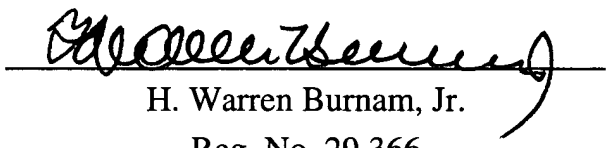
In view of the foregoing and other considerations, all claims are deemed in condition for allowance. A formal indication of allowability is earnestly solicited.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application, including but not limited to claims fee, extension of time fees, and Information Disclosure Statement (IDS) fees.

Should the Examiner feel that an interview with the undersigned would facilitate allowance of this application, the Examiner is encouraged to contact the undersigned.

Respectfully submitted,
NIXON & VANDERHYE P.C.

September 6, 2005

By: 
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